

FIG. 1

(PRIOR ART)

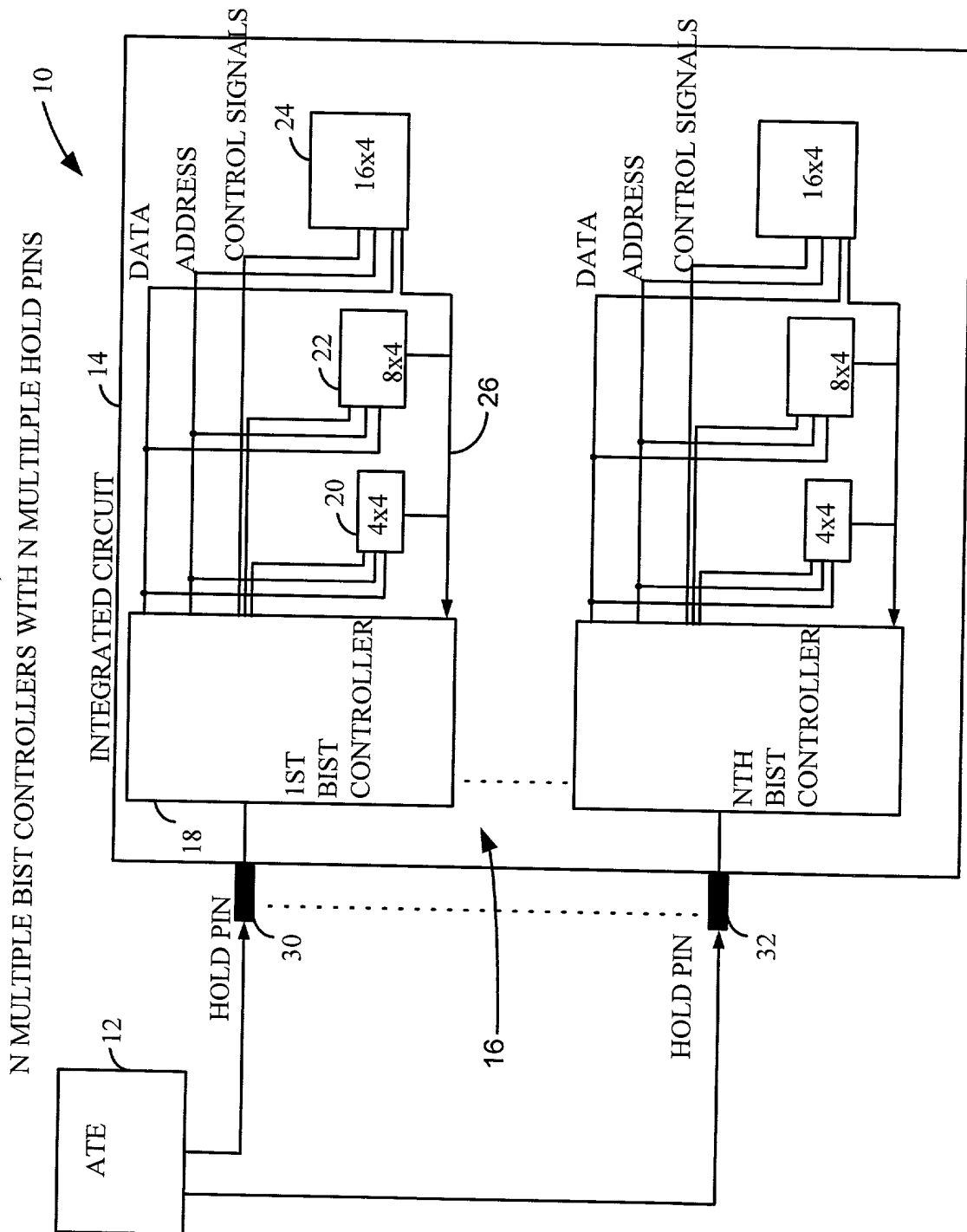


FIG. 2

TEST ON THREE MEMORIES COUPLED TO A SINGLE SEQUENTIAL BIST
CONTROLLER USING THREE SEPARATE IDLE PERIODS

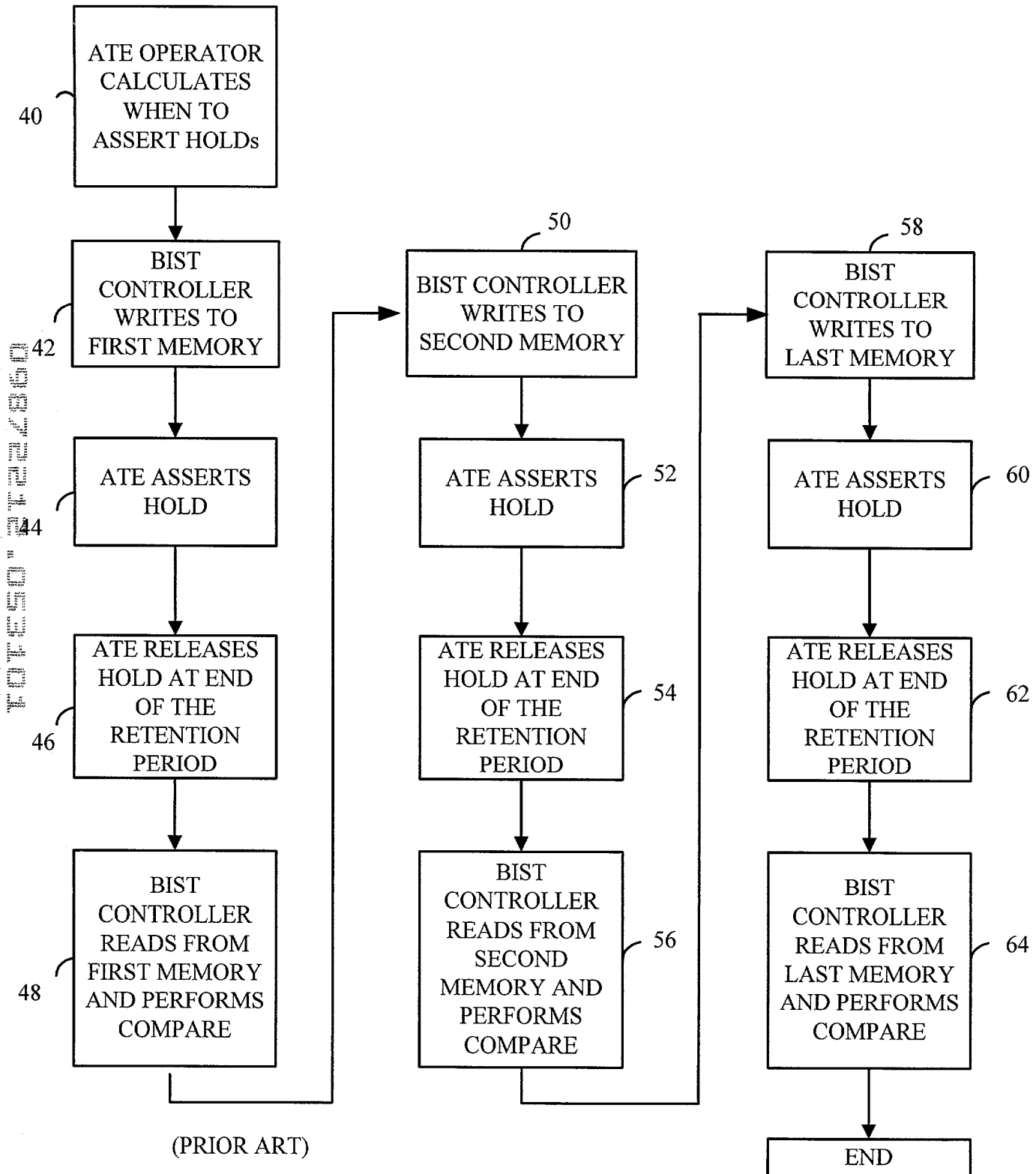


FIG. 3

N MULTIPLE BIST CONTROLLERS WITH SINGLE SYNCHRONIZE AND RESUME PINS

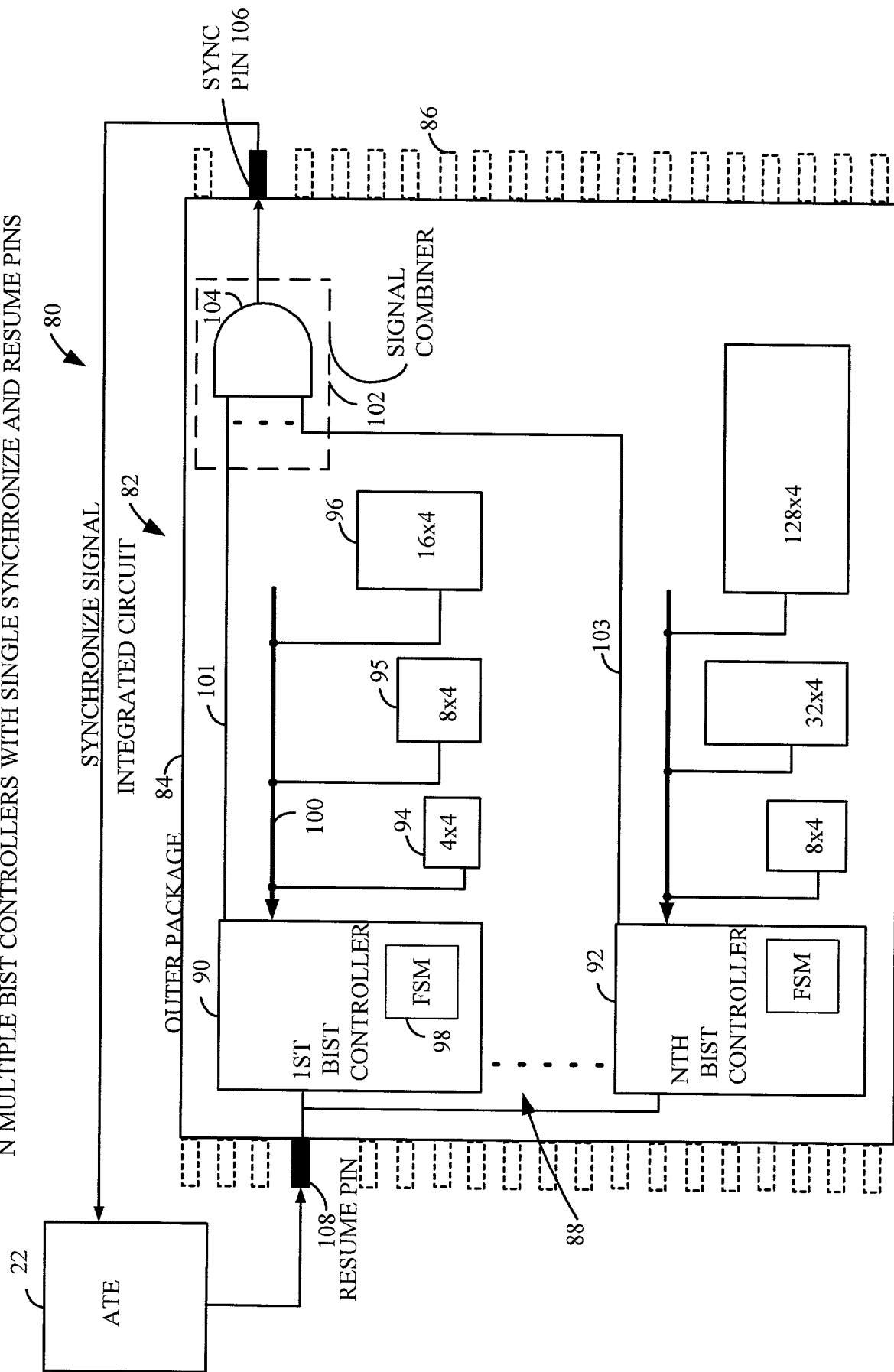


FIG. 4

TEST OF MEMORIES WITH MULTIPLE PARALLEL BIST
CONTROLLERS USING SYNCHRONIZATION STATE

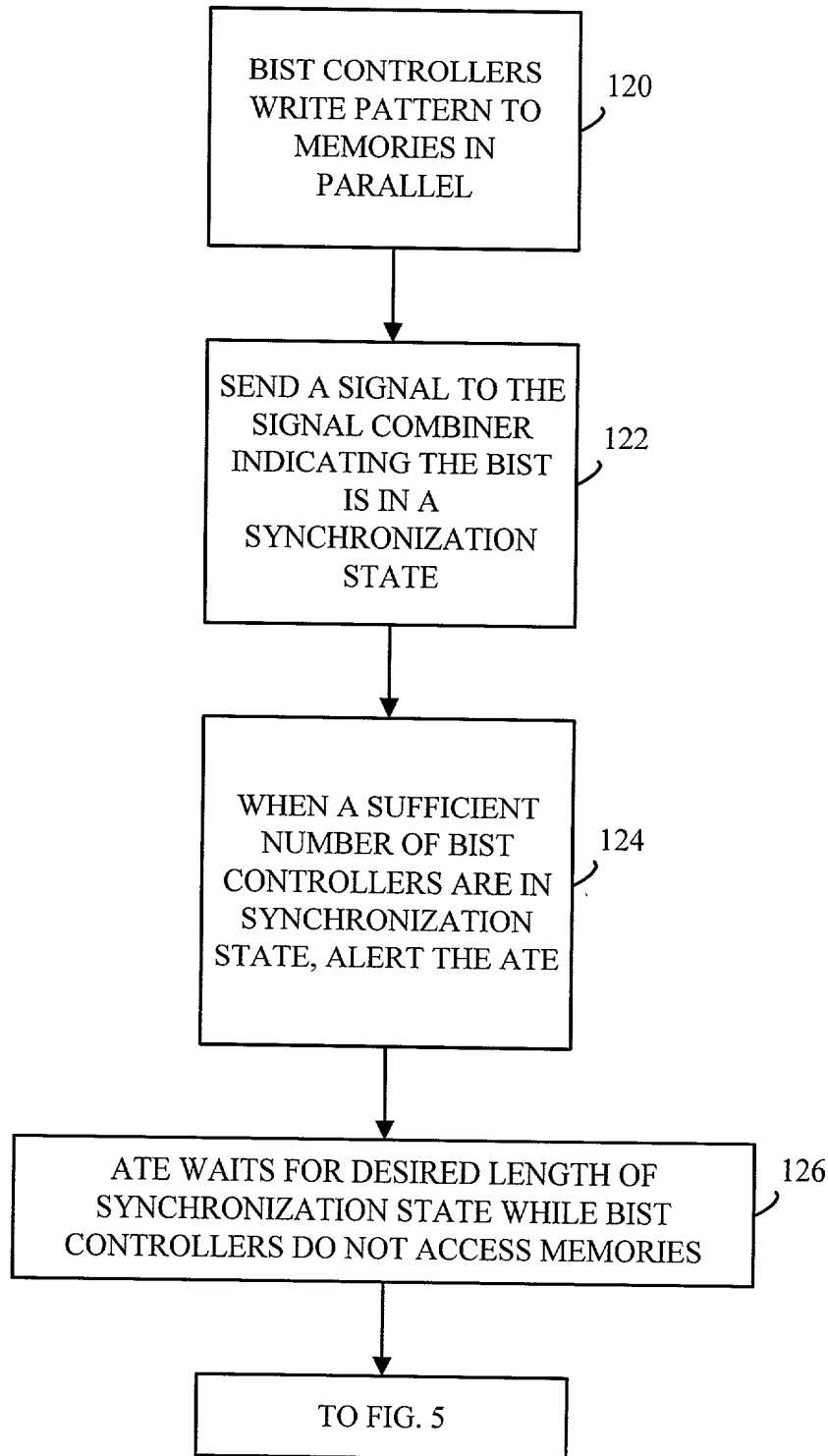


FIG. 5

TEST OF MEMORIES WITH MULTIPLE PARALLEL BIST
CONTROLLERS USING SYNCHRONIZATION STATE (CONTINUED)

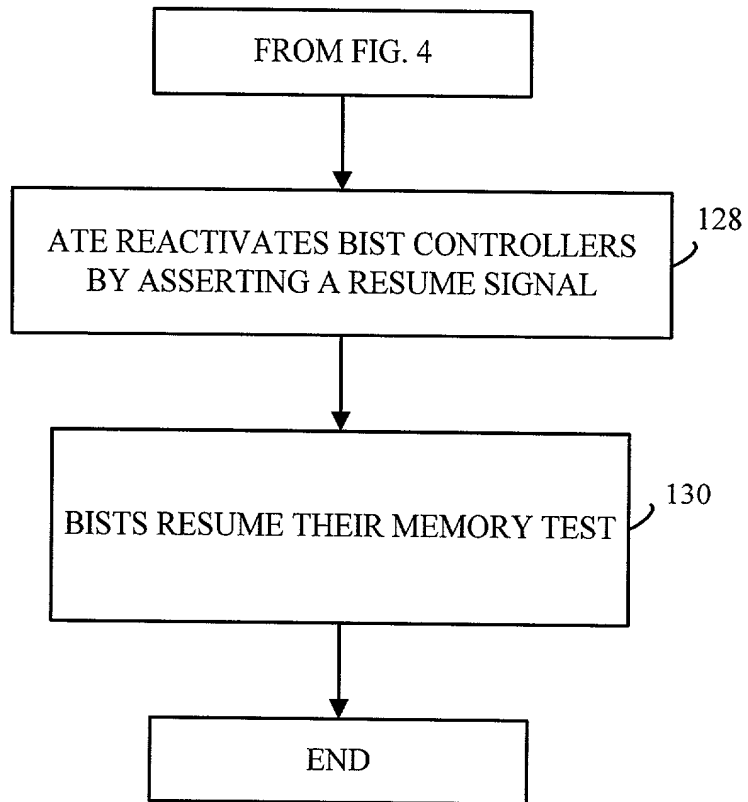


FIG. 6

TEST OF MEMORIES WITH MULTIPLE SEQUENTIAL BIST
CONTROLLERS USING SYNCHRONIZATION STATE

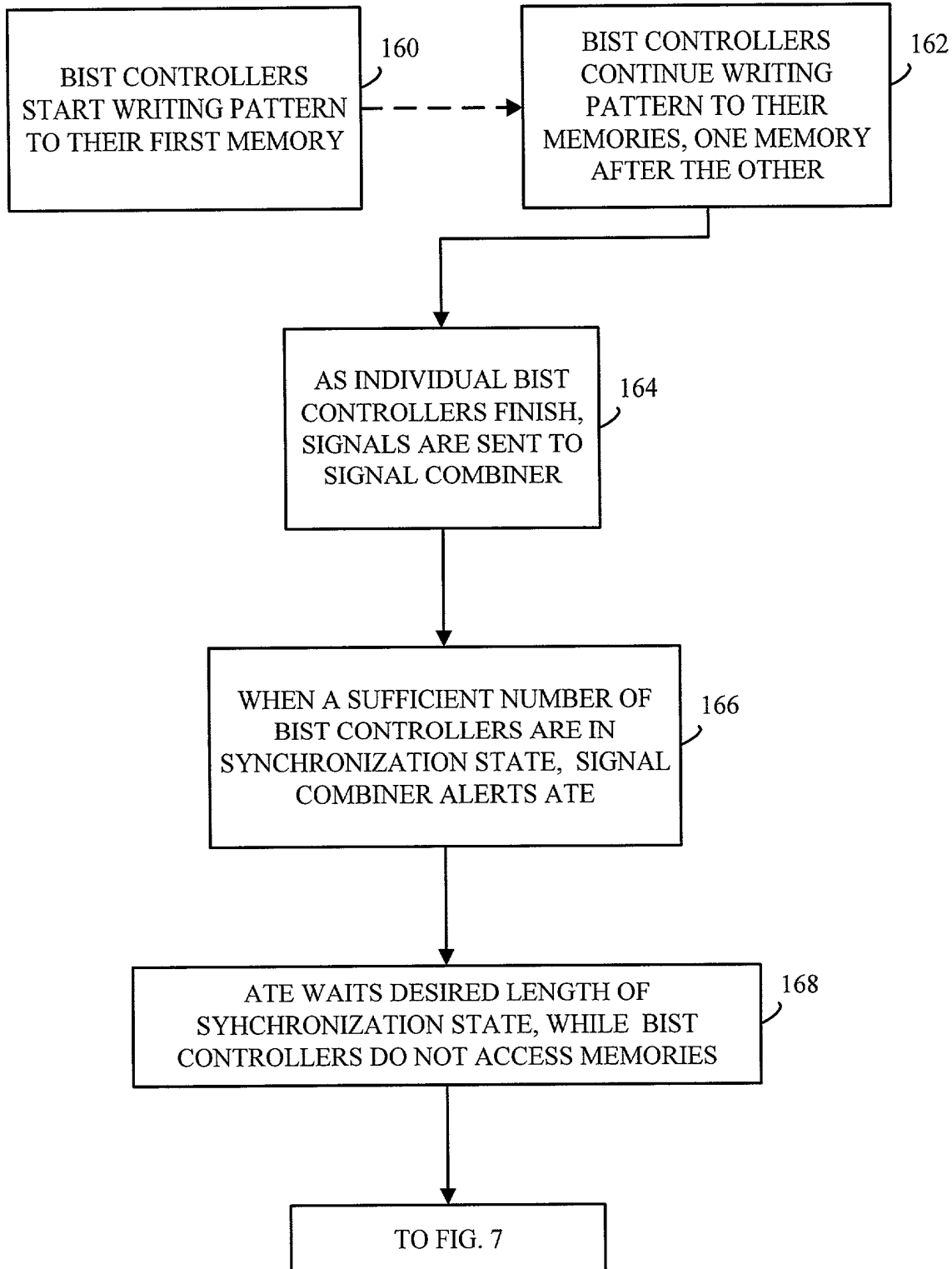


FIG. 7

TEST OF MEMORIES WITH MULTIPLE SEQUENTIAL BIST
CONTROLLERS USING SYNCHRONIZATION STATE (CONTINUED)

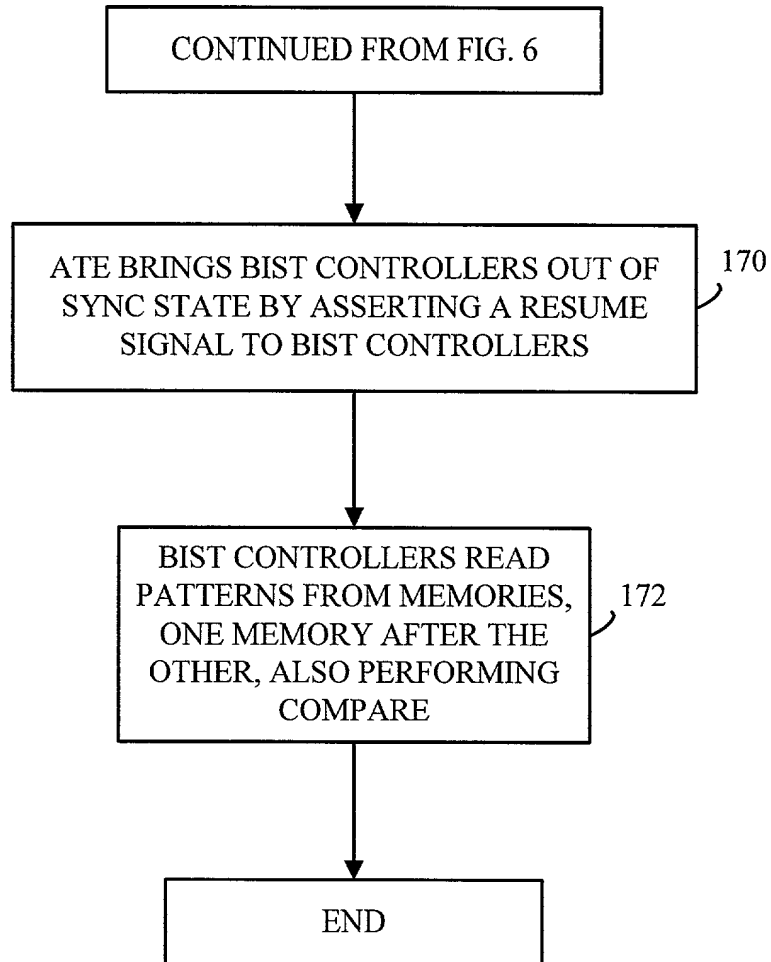


FIG. 8 — BIST CONTROLLER GENERATOR

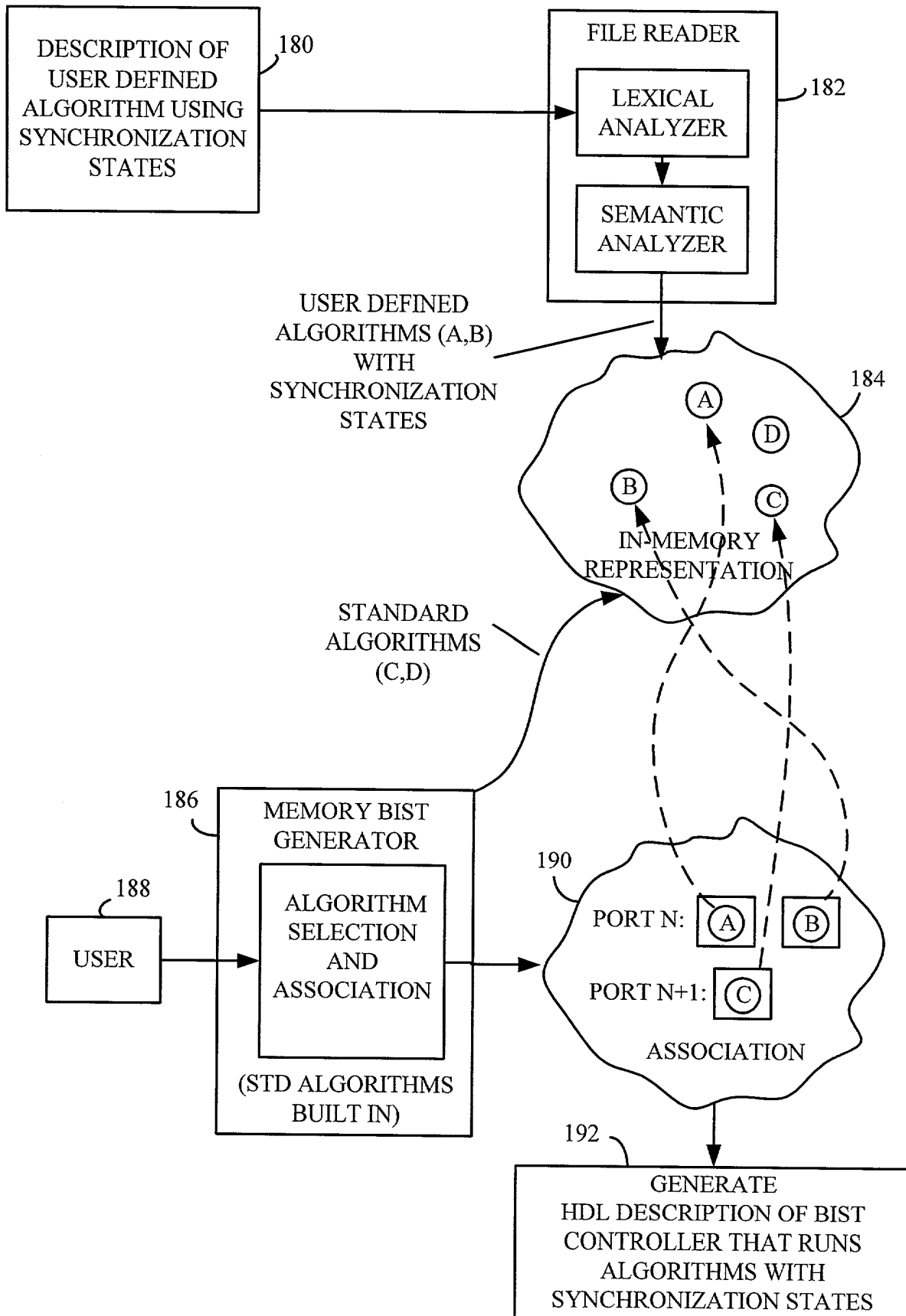


FIG. 9

GENERATING A BIST CONTROLLER THAT RUNS USER
DEFINABLE ALGORITHMS WITH SYNC KEYWORD

